10/600,222

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Express Mail Label No. Dated: _____

Docket No.: 08211/000S135-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Bumha Lee et al.

Patent No.: 6,759,975 B1

Issued: July 6, 2004

For: DIGITAL-TO-ANALOG CONVERTER WITH A SHIFTED OUTPUT AND AN INCREASED RANGE

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted an error which should be corrected.

In the Specification:

Column 2, Line 2 Delete "Mathew" and insert -- Matthew --.

Column 4, Line 13, Delete "11" and insert -- I1 --.

Column 10, Line 1, In Claim 19, after "providing" insert -- the second current to an --.

Column 10, Line 2, In Claim 19, after "and" insert -- wherein--.

Column 10, Line 6, In claim 20, after "providing" insert --the --.

The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find copies of pages 6 & 15.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: May 16, 2005

Respectfully submitted,

By _____

Flynn Barrison
Registration No.: 53,970
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

The Commissioner is authorized to charge any deficiency or credit any excess in this fee to Deposit Account No. 04-0100.

PTO/SB/44 (04-05)
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,759,975 B1
APPLICATION NO.	:	10/600,222
ISSUE DATE	:	July 6, 2004
INVENTOR(S)	:	Bumha Lee et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 2, Line 2 Delete "Mathew" and insert -- Matthew --.

Column 4, Line 13, Delete "11" and insert -- I1 --.

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Column 10, Line 6, In claim 20, after "providing" insert --the --.

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MAILING ADDRESS OF SENDER:
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

MAY 2 4 2005

Application No. (if known): 10/600,222 Attorney Docket No.: 08211/000S135-US0

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Registration Number, if applicable

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current mirror load. Transistor M6 is configured to operate as a cascode transistor in cooperation with transistor M8. Transistor M7 is configured to operate as a cascode transistor in cooperation with transistor M9. Current source circuit I1 is configured to provide a tail current to OTA 204.

Resistance circuit R3 is arranged to bias cascode transistors M6 and M7. The current through resistance circuit R3 (I_{R3}) is approximately given by I1/2, such that the voltage between nodes N328 and N330 is approximately given by R3*(I1/2). The voltage at node N332 is approximately equal to V_{HI}-V_{GS}, where V_{GS} is the gate-to-source voltage of transistor M8 (or M9). The voltage at node N328 is approximately given by V_{HI}-V_{GS}-R3*(I1/2). The resistance of resistance circuit R3 is selected to provide an appropriate bias voltage to cascode transistors M6 and M7.

Transistor M3, current source I2, and current source I3 are arranged in cooperation to bias cascode transistors M4 and M5. Transistors M1 and M3 have a common source at node N332. Transistor M3 is configured such that the V_{GS} of transistor M3 is greater than the V_{GS} of transistor M1. For example, transistor M3 may have a long channel length and a short channel width such that the V_{GS} of transistor M3 is relatively large. Current source I2 and current source I3 are each configured to produce approximately the same current. Current source I3 is arranged to operate such that the current that is provided by current source I3 is sourced from V_{DD}.

Many alternative embodiments of OTA circuit 202 are possible. For example, current sources I1 and I2 may combined into one current source. Current source I3 may be replaced with an alternative kind of current-limiting device, such as a resistor. Resistance circuit R3 may be replaced with an alternative circuit that is configured to bias cascode transistors M6 and M7. Transistor M3 may be replaced with an alternative circuit that is configured to bias cascode transistors M4 and M5.

FIG. 4 is an illustration of an example embodiment of a current digital-to-analog converter circuit (204) that is configured for operation in DAC circuit 104. Circuit 204 includes transistors (M10-M17), a resistance circuit (R4), and an amplifier circuit (AMP1). Amplifier circuit A1 has a noninverting input that is coupled to node N118, an inverting input that is coupled to node N430, a first power supply input that is

19. The method of Claim 16, wherein converting the sum is accomplished via a resistance circuit that is coupled between the sense node and the second supply node, and wherein coupling the second current to the sense node comprises providing the second current to an output node, wherein the analog voltage is associated with the output node, and wherein the output node is coupled to the sense node via another resistance circuit that is coupled between the output node and the sense node.

20. The method of Claim 16, wherein providing the second current comprises providing the second current such that the second current is approximately proportional to the difference between the reference voltage and the sense voltage.